REMARKS

This responds to the Office Action mailed on February 24, 2005.

Claims 2, 4, 13, 16-18, 21, and 25 are amended, claim 19 is canceled, and claims 26-28 are added; as a result, claims 1-18 and 20-28 are now pending in this application.

Objection to the Drawings

The Examiner objected to the drawings because they fail to label the reference numerals according to their functions. Specifically, the Examiner objected to FIG. 4 (the Office Action referes to "reference numeral 404 in Fig. 9", but Applicant's believe that the Examiner meant Fig. 4, because reference numeral 404 appears in Fig. 4). Applicant has added corresponding textual labels within the blocks corresponding to reference numerals 402, 404, 406, 408, 410, and 412 of FIG. 4. Support for the label additions may be found in the specification at page 8, line 29 through page 9, line 3. Applicant believes that the replacement of FIG. 4 overcomes this objection, and respectfully requests that it be withdrawn. In the event that the replacement of FIG. 4 does not fully overcome the objection, Applicant requests that the Examiner kindly indicate which additional figures and/or blocks should be similarly modified, and Applicant will do so in a future communication.

§112 Rejection of the Claims

Claims 17-19 were rejected under 35 USC § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. Applicant has canceled claim 19, and has amended claims 17 and 18 in order to specify structural cooperative relationships of elements. Accordingly, Applicant believes that the rejection of claims 17 and 18 under 35 USC § 112 has been overcome, and that the rejection of claim 19 is now moot. Applicant respectfully requests that the rejection of claims 17-19 be reconsidered and withdrawn. Support for the amendments to claims 17 and 18 can be found in the originally-filed figures and specification at Figure 2, and page 6, line 19 through page 7, line 15.

IN THE DRAWINGS

A corrected drawing sheet is supplied herewith, and is labeled as "REPLACEMENT SHEET". Specifically, a corrected drawing sheet that includes FIG. 4 is included herewith. The differences between the previously-filed drawing sheet and the corrected drawing sheet is that the blocks corresponding to reference numerals 402, 404, 406, 408, 410, and 412 now include a corresponding textual label in addition to the reference numerals.

§103 Rejection of the Claims

Claims 1, 5, 6, 12, 14, 15, 20 and 22-24 were rejected under 35 USC § 103(a) as being unpatentable over Saeki (U.S. 6,621,317) in view of Ooishi (U.S. 6,424,585). Applicant respectfully traverses the rejection.

Saeki discloses a phase adjustment circuit 101, which receives an input clock and generates an output clock having a phase adjusted with respect to a reference clock. (Fig. 1, col. 8, line 59-64). The phase adjustment circuit 101 may include an interpolator. (col. 9, lines 1-3).

Referring to Fig. 20, an embodiment of a phase adjustment circuit 101 includes an interpolator 10, a switch (rotary switch) 20, a fine adjustment interpolator 30, and a control circuit 40. (col. 19, lines 55-61). The interpolator 10 produces multiple-phase frequency-multiplication clocks P0 to Pn from an input clock. The rotary switch 20 selects two neighboring clocks of the multiple-phase frequency-multiplication clocks P0 to Pn to furnish as two input signals to the fine adjustment interpolator 30. The fine adjustment interpolator 30 outputs, based on a control signal, a signal of a phase corresponding to the internal division of the phase difference of the two inputs. (Fig. 20, col. 19, line 62 through col. 20, line 17).

Ooishi discloses a structure of an internal voltage down converter for down-converting an external power supply voltage to generate an internal power supply voltage. (col. 1, lines 16-23). In particular, Fig. 22, which was cited in the Office Action as disclosing "a circuit having function of a current source select signal generator circuit . . ." illustrates a voltage drop means forming a portion of an internal power supply voltage generation circuit. (Figs. 16, 22, and col. 22, lines 1-4).

Applicant's claims 1, 5, 6, 12, 14, 15, 20, and 22-24 are distinguishable from that which is disclosed in Saeki, Ooishi, or their combination, in that Applicant's claims include at least the following distinguishable features:

> ". . . a delay chain, which is capable of receiving an input signal and producing multiple delayed signals that represent delayed versions of the input signal, wherein the multiple delayed signals are separated by a first phase increment;
>
> multiple interpolator blocks, operably coupled to the delay chain, wherein consecutive ones of the multiple interpolator blocks are capable of receiving and interpolating between consecutive ones of the multiple delayed signals to produce an

interpolated version of the input signal, wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment . . ." (claims 1, 5, 6, 12, 14, 15, 20 and 22)

OR

". . . generating current source select signals using a split current source;

receiving, by two consecutive interpolator blocks, two consecutive multi-phase signals, wherein the two consecutive multi-phase signals are separated by a first phase increment; and

interpolating between the two consecutive multi-phase signals by varying a first current produced by a first block of the consecutive interpolator blocks, and a second current produced by a second block of the consecutive interpolator blocks . . ." (claims 23-24)

Saeki and Ooishi, when combined, must teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)). However, Saeki and Ooishi do not teach or suggest all the claim elements. Notably, Saeki does not disclose *multiple* interpolators capable of receiving and interpolating between consecutive ones of multiple delayed signals. Instead, Saeki discloses a rotary switch to select two neighboring clocks, and exactly one fine adjustment interpolator 30 to interpolate between the clocks. Ooishi does not add anything to address this distinguishing feature.

Further, there is no suggestion in Saeki or Ooishi to combine the references. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01.

Additionally, Ooishi is non-analogous art. Analogous art is all art that is either in the field of technology of the claimed invention or deals with the same problem solved by the claimed invention even though outside the field of technology. *In re Wood*, 599 F.2d 1032, 202 USPQ 171 (CCPA 1979). Ooishi describes a structure of an internal voltage down converter. In contrast, claims 1, 5, 6, 12, 14, 15, 20 and 22 recite a circuit having a delay chain and multiple

interpolator blocks. Thus, Ooishi is not analogous art because it is not in the field of technology of the claimed invention, nor does it deal with the same problem solved by the claimed invention.

The rejection of claims 23-24 under 35 USC § 103(a) was not specifically addressed in the Office Action. If this rejection is repeated, Applicant respectfully requests that the Examiner include citations within the references (e.g., Saeki and Ooishi), which disclose the limitations of claims 23-24.

For the above reasons, Applicant believes that the rejection of claims 1, 5, 6, 12, 14, 15, 20 and 22-24 under 35 USC § 103(a) has been overcome. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection, and allow claims 1, 5, 6, 12, 14, 15, 20, and 22-24.

Allowable Subject Matter

Claims 2-4, 13, 16, 21 and 25 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended claims 2 (from which claim 3 depends), 4, 13, 16, 21, and 25. Applicant believes that these amendments overcome the objection, and respectfully request that the Examiner withdraw the objection and allow claims 2-4, 13, 16, 21, and 25.

Claims 7-11 were allowed. Applicant appreciates the Examiner's careful consideration of and allowance of these claims.

New Claims 26-28

New claims 26-28 are derived from originally filed claims 1 and 2. No new matter is introduced as a result of these claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Sherry Schumm at (480) 538-1735 or Applicant's below-named representative at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

BHEEM PATEL ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date May 24, 2005

By Ann M. McCrack.
Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of May, 2005.

Dennis J. Kanyk
Name

Signature